Claims

1. A method of adjusting equalization parameters in a receiver comprising
an analog filter,
a clock recovery unit (CR),
an equalizer including error correction means and
adaption means (AD),
the method including the steps of:
receiving a data stream which has data blocks with an information section and an error correction section,
measuring a bit error rate (BER) from the number of corrected bits in the data block,
changing a predetermined equalization parameter,
measuring the bit error rate (BER) after change of the predetermined parameter,
changing the predetermined equalization paramter with an amount and in a direction so as to lower the bit error rate (BER),
continuing with measuring the bit error rate (BER) and changing the predetermined equlizing parameter until an optimum is reached.

The method of claim 1, for adjusting the threshold value of the receiver,
wherein the history of occurring of the bits preceding the actual sampled bit is taken into consideration in that the amount and direction of adjustment is derived from a look-up table or a circuit forming a look-up table.

The method of claim 2,
wherein the previous bit (0 or 1) in the history of occurring of the bits preceding the actually sampled bit, is taken into consideration in that the receiver threshold (th) is decreased when the previous bit is 0, and is increased when the previous bit is 1.

The method of claim 1

wherein incoming data are converted into digital form and subdivided into blocks which are processed for error correction and adjustment of equalization parameter.

2. A receiver adapted to adjust equalization parameters thereof, comprising

an analog data input with filter;

an equalizer including

a threshold decision circuit (TH) acting as an analog-digital converter;

a clock recovery unit (CR);

means for passing the digital data stream through the receiver to data output (DO);

an error correction means (FEC);

a feed back loop having adaption means (AD) for adjusting parameters of the equalizer;

characterized in that

the error correction means (FEC) includes means for forming a bit error rate (BER),

and in that

the adaption means (AD) has means for dithering parameters of the receiver.

3. A receiver for adjusting the threshold value thereof, comprising

an analog data input (DI);

a threshold decision circuit (TH) acting as an analog-digital converter;

a clock recovery unit (CR);

means (SR) for passing the digital data stream through the receiver to data output (DO);

an error correction means (FEC);

a feed back loop having adaption means (AD) for adjusting parameters of the equalizer,
characterized in that
the feedback loop includes a circuit in the kind of a look-up table which, based upon a bit error rate (BER) and tap means (TM) in the digital data passing means (SR), provides signals indicating the amount and direction of adjustment of the receiver threshold (th).

4. The receiver of claim 6
wherein the tap means (TM) include a flip-flop (FF) for providing the value of the previous bit preceding the actual sampled bit, the look-up table circuit increasing or decreasing the value of the receiver threshold (th) for the actual received data bit.

5. The receiver of claim 6
wherein the tap means (TM) include flip-flops (FF) in series and gate circuits so as to detect the direction of signal transitions (0/1 and 1/0), a pair of conditional counters (CC1, CC2; CC3, CC4) being assigned to each signal transition (0/1 and 1/0),
one conditional counter of the pair sums the number of the corrected bits of one value (1), and the other counter sums the number of the corrected bits of the other value (0),
the summed numbers of the counters being supplied to each an integrator (NL 1, NL 2) which provides the adjustment value to the threshold decision circuit (TH).